REMARKS

In response to the Office Action mailed on November 22, 2006, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has amended claims 6, 7 and 10-15. Claims 6, 7 and 10-15 are pending in the application.

Rejection of claims under 35 USC §102

Claims 6, 10, 11 and 12 have been rejected under 35 USC §102 as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claims.

In claim 6, a single identifier (mask) is used for all of the control words of the sequence. This is in contrast to the Tanaka reference in which a separate bit-mask is used for each control word. For example, FIG. 6 of Tanaka shows 5 masks, one for each of the 5 control words (see 720 for example). The approach of Tanaka allows for higher compression, but requires more complex hardware for execution. In addition, more memory is required to store the bit-masks.

In claim 6, as previously filed, a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of a plurality of control words. That is, a bit of the identifier corresponding to a first datapath element is set only if the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words. In contrast, Tanaka has a mask for each control word. Applicant submits that the mask of Tanaka is not equivalent to the identifier of claim 6.

Claim 6 has been amended to clarify that a bit of the identifier corresponding to a first datapath element is set only if the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words. The scope of the claim is not altered by this amendment, since the meaning was implicit in the claim before amendment, which referred to the 'corresponding ordered field'. Referring to Fig. 1 of the application, the mask (identifier) contains a zero if and only if the all of the fields in the column above it are NOP instructions.

The fields in one column are all processed by the same datapath element (see page 7, lines 1-11 of the specification, for example). Thus column 3, which contains the instructions for datapath element 3, contains all NOP's, and so the third bit of the identifier is set to zero. In contrast, column 2, which contains the instructions for datapath element 2, contains 3 NOP's but the instruction in field 2 of VLIW 1 is not a NOP instruction, and so the second bit of the identifier is not set to zero.

In Tanaka there are four fields (the columns in table 700 of FIG. 6) corresponding the four clusters A, B, C and D. No column contains all NOP instructions. If the method of claim 1 were applied, the results would a single 4-bit identifier (one bit for each processing element or cluster). The single identifier for the whole sequence would have value 1111, since no column contains a NOP in every word of the sequence. Thus, no datapath element would be disabled since every cluster is used at least once when the sequence of control words is executed. In contrast, Tanaka has a 4-bit mask for every word of the sequence, i.e. a 20-bit mask and NOPs are removed even though every cluster is used in the sequence.

In an interview with the examiner on March 16th, 2007, the examiner agreed that the bit masks of Tanaka were not equivalent to a single identifier that is set only if the ordered field corresponding to a datapath element contains a NOP instruction in every control word of a sequence of control words, as called for in the amended claim 6. Applicant submits that this feature of the claim was implicit in the claim before amendment.

Claim 6 also calls for the disabled datapath elements to remain disabled while the sequence of instructions is processed. Thus, the hardware is configured only once before processing of the sequence begins. This is in contrast to Tanaka where the hardware is reconfigured for each control word, dependent upon both bit masks and cache hits. This is disadvantageous, since the process of reconfiguring the hardware consumes processor power. However, power consumption is not a primary concern for Tanaka, since his objective is to minimize amount of cache memory used. Tanaka uses a mask for every control word, and so processor elements must be controlled as each word is processed. This requires more logic circuit, which, in turn, consumes

power. This may not be a problem when memory reduction is the aim, but it is counter productive if power reduction is the aim.

A NOP is an instruction that does not change the state of the processor. The Applicant submits that executing a NOP instruction is not equivalent to disabling a datapath element. An analogy would be a signal amplifier. An amplifier may be switched on (powered) but have no input or output signals (i.e. is not operating, but is capable of operation), but this is not equivalent to switching the amplifier off (when is incapable of operating).

Claim 6 has been further amended to clarify that an 'element of the processor' refers to a datapath element, as taught in the specification.

Claim 6 has been still further amended to emphasize the tangible result of the method, which is a reduction in the power consumed by the processor. This result was previously specified in the second element of claim 6, which read 'disabling an element of the processor, to reduce power consumption by the processor,…'.

In light of the foregoing amendments and remarks, Applicant respectfully submits that the Tanaka reference does not teach, suggest, disclose or otherwise anticipate the recitations of claim 6. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for claim 6 be mailed at the Examiner's earliest convenience.

Claims 10 has been rejected under 35 USC §102 as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claim.

As described above with reference to claim 6, Applicant submits that the mask of Tanaka is not equivalent to the mask of claim 10.

In claim 10, a single mask is used for all of the control words of the sequence. This is in contrast to the Tanaka reference in which a separate bit-mask is used for each control word. For example, FIG. 6 of Tanaka shows 5 masks, one for each of the 5 control words (see 720 for example). The approach of Tanaka allows for higher compression, but requires more

complex hardware for execution. In addition, more memory is required to store the bit-masks.

In claim 10, as previously filed, a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of a plurality of control words. That is, a bit of the identifier corresponding to a first datapath element is set only if the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words. In contrast, Tanaka has a mask for each control word.

Claim 10 has been amended to clarify that a bit of the identifier corresponding to a first datapath element is set only if the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words. The scope of the claim is not altered by this amendment, since the meaning was implicit in the claim before amendment, which referred to the 'corresponding ordered field'.

In an interview with the examiner on March 16th, 2007, the examiner agreed that the bit masks of Tanaka were not equivalent to a single identifier that is set only if the ordered field corresponding to a datapath element contains a NOP instruction in every control word of a sequence of control words, as called for in the amended claim 10. Applicant submits that this feature of the claim was implicit in the claim before amendment.

Claim 11 has been rejected under 35 USC §102 as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claim.

Claim 11 depends from claim 10, discussed above. In claim 11, the memory banks are disabled if they are unused for the whole sequence of control words. The memory banks remain disabled while the sequence of control words is processed. In contrast, Tanaka does not disable memory banks, rather, he uses a selector, 430 in FIG. 14 for example, to read a cache output or to insert a NOP. The cache 430 is unused if a NOP is inserted, but Tanaka does not teach that it is disabled. Further, Tanaka uses a mask for every control word, so the processor is reconfigured every control word,

whereas the configuration of the system of claim 11 remains unchanged during complete sequence, since only one mask is utilized.

Claim 12 has been rejected under 35 USC §102 as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claim.

Claim 12 depends from claim 10, discussed above. In claim 12, the datapath elements are disabled if they are unused for the whole sequence of control words. The memory banks remain disabled while the sequence of control words is processed. In contrast, Tanaka does not disable datapath elements, as discussed above with reference to claim 6.

Rejection of claims under 35 USC §103

Claim 13 has been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Pechanek (Patent No. US 6,173,389). Applicant respectfully traverses this rejection of the claim.

Claim 13 depends from claim 12 discussed above. Applicant submits, in light of the foregoing discussion of claim 10, that even if one were to combine the Tanaka reference with the Pechanek reference, the result would not be the claimed invention of claim 13. Tanaka does not teach a system in which datapath elements are disabled for execution of a complete sequence of control words. This defect is not cured by the Pechanek reference.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Pachanek references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 13 be mailed at the Examiner's earliest convenience.

Claims 7 and 14 has been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Shebanow

(Patent No. US 5,367,494). Applicant respectfully traverses this rejection of the claim.

Claim 7, which depends from claim 6, introduces the further limitation of disabling a memory bank associated with a datapath element if every control words in the sequence contains a NOP in the field corresponding to the datapath element associated with the memory bank. This is not taught by Tanaka, in particular Tanaka does not teach a system in which datapath elements and memory banks are disabled during execution of a complete sequence of control words.

The examiner suggests that the use of Shebanow could provide Tanaka with the ability to accept and send data from a plurality of memory sets at a given cycle. However, claim 7 teaches that datapath elements and memory banks are disabled for execution of a complete sequence of control words. The disablement is controlled by an identifier having one bit for each datapath element of the processor, wherein a bit of the identifier corresponding to a first datapath element is set only if the ordered field corresponding to the first datapath element contains a NOP instruction in every control word of the sequence of control words.

Similarly, in claim 14 datapath elements and memory banks are disabled before the sequence of control word is processed. In Tanaka, each control word and its associated mask is processed separately. Thus the configuration is altered as the sequence of control word is processed.

Claim 14 has been amended to recite, explicitly, that the claimed system operates with reduced power consumption.

Claim 15 depends from claim 14 discussed above. The defects in the Tanaka reference are not cured by the addition of the Shebanow and/or Pachanek reference.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka, Shebanow and Pachanek references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim. Applicant thus respectfully requests that this basis of

rejection of the claim be withdrawn and that a Notice of Allowance for claims 7 and 14 be mailed at the Examiner's earliest convenience.

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 6, 7 and 10-15 have been overcome. The scope of the amended claims is substantially the same with implicit meaning now made explicit. Allowance of claims 6, 7 and 10-15 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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